WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

a plurality of electrodes provided for an operating region formed in the substrate;

a plurality of electrode pads formed on the substrate and each connected to a corresponding electrode of the operating region;

a plurality of wiring connections between one of the electrodes and a corresponding electrode pad; and

a protecting element formed along each of the wiring connections and comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region between the first and second high concentration impurity regions, the protecting element being connected between two electrodes of the plurality of electrodes.

2. A semiconductor device comprising:

a substrate;

a gate electrode, a source electrode and a drain electrode, each of the electrodes being provided for an operating region formed in the substrate;

an electrode pad provided for each of the electrodes and formed on the substrate;

a plurality of wiring connections between one of the electrodes and a corresponding electrode pad; and

a protecting element formed along each of the wiring connections and comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region between the first and second high concentration impurity regions, the protecting element being connected between two of the gate, source and drain electrodes.

3. The semiconductor device of claim 1 or 2, wherein the protecting element is configured to improve an electrostatic breakdown voltage of the semiconductor device by at least 20 volts over the semiconductor device without the protecting element.

4. The semiconductor device of claim 1 or 2, wherein each of the protecting elements

is disposed adjacent one of the electrode pads.

5. The semiconductor device of claim 1 or 2, wherein one of the first and second high concentration impurity regions is connected to part of one of the electrode pads or part of a metal wiring connection connected to one of the electrodes.

6 The semiconductor device of claim 1 or 2, wherein one of the first and second high concentration impurity regions is connected to one of the wiring connections.

7. The semiconductor device of claim 1 or 2, further comprising a third high concentration impurity region disposed at a periphery of one of the electrode pads, wherein one of the first and second high concentration impurity regions comprises part of the third high concentration impurity region.

8. The semiconductor device of claim 1 or 2, wherein one of the wiring connections comprises a resistor.

9. The semiconductor device of claim 1 or 2, wherein one of the first and second high concentration impurity regions comprises part of one of the wiring connections.

10. A semiconductor switching device comprising:

a first field effect transistor and a second filed effect transistor each formed on a substrate, each of the transistors comprising a source electrode, a gate electrode and a drain electrode,

a common input terminal connected to the source electrodes or the drain electrodes of the first and second transistors;

a first output terminal provided for the first transistor and a second output terminal provided for the second transistor, each of the output terminals being connected to a corresponding source or drain electrode that is not connect to the common input terminal;

a first control terminal provided for the first transistor and a second control terminal provided for the second transistor, each of the control terminals being connected to a

corresponding gate electrode to make one of the first and second transistors turn on according to a control signals applied to the control terminals;

an electrode pad provided for each of the terminals and formed on the substrate;

a plurality of wiring connections between the gate electrode of at least one of the first and second transistor and the electrode pad of the corresponding control terminal; and

a protecting element formed along each of the wiring connections and comprising a first high concentration impurity region, a second high concentration impurity region and an insulating region between the first and second high concentration impurity regions, the protecting element being connected between the gate and source electrodes of the corresponding transistor or the gate and drain electrodes of the corresponding transistor or both.

11. The semiconductor switching device of claim 10, wherein the protecting element is configured to improve an electrostatic breakdown voltage of the semiconductor switching device by at least 20 volts over the semiconductor device without the protecting element.

12. The semiconductor switching device of claim 10, wherein the two protecting elements are disposed adjacent the electrode pads of the common input terminal and the first output terminal respectively or adjacent the electrode pads of the common input terminal and the second output terminal respectively.

13. The semiconductor switching device of claim 10, wherein one of the first and second high concentration impurity regions is connected to part of one of the electrode pads or part of a metal wiring connection connected to one of the electrodes.

14. The semiconductor switching device of claim 10, wherein one of the first and second high concentration impurity regions is connected to one of the wiring connections.

15. The semiconductor switching device of claim 10, further comprising a third high concentration impurity region disposed at a periphery of the electrode pad of the common input terminal or the first output terminal or the second output terminal, wherein one of the first and second high concentration impurity regions comprises part of the third high concentration

impurity region.

16. The semiconductor switching device of claim 10, wherein one of the wiring connections comprises a resistor.

17. The semiconductor switching device of claim 10, wherein one of the first and second high concentration impurity regions comprises part of one of the wiring connections.

18. The semiconductor switching device of claim 10, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and a width of the first impurity region is smaller than a width of the second impurity region so that upon discharging of an electrostatic energy through the protecting element a first current path for electron or hole is formed in the insulating region between opposing faces of the first and second high concentration impurity regions and between bottom faces of the first and second high concentration impurity regions and that a second current path for electron or hole is formed in the insulating region between the bottom face of the second high concentration impurity region and another side face of the fist high concentration impurity region, the second current path being deeper than the first current path.

19. The semiconductor switching device of claim 18, wherein the first high concentration impurity region is connected to an extension part so that upon discharging of the electrostatic energy through the protecting element a third current path for electron or hole is formed in the insulating region between the extension part and the second high concentration impurity region.

20. The semiconductor switching device of claim 10, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and a width of the first impurity region is substantially equal to a width of the second impurity region so that upon discharging of an electrostatic energy through the protecting element a first current path for electron or hole is formed in the insulating region between opposing faces of the first and second high concentration impurity regions and between bottom faces of the first and second high

concentration impurity regions and that a second current path for electron or hole is formed in the insulating region between the another side face of the second high concentration impurity region and another side face of the fist high concentration impurity region, the second current path being deeper than the first current path.

21. The semiconductor switching device of claim 20, wherein the first high concentration impurity region is connected to an extension part so that upon discharging of the electrostatic energy through the protecting element a third current path for electron or hole is formed in the insulating region between the extension part and the second high concentration impurity region.

22. The semiconductor switching device of claim 21, wherein the second high concentration impurity region is connected to an extension part so that upon discharging of the electrostatic energy through the protecting element a third current path for electron or hole is formed in the insulating region between the extension part and the first high concentration impurity region.

23. The semiconductor switching device of claim 18 or 20, wherein the width of the first high concentration impurity region is 5 μm or smaller.

24. The semiconductor switching device of claim 18 or 20, wherein a conductivity modulation efficiency of the second current path is at least 5 times higher than a conductivity modulation efficiency of the first current path of the protecting element without the second current path.

25. The semiconductor switching device of claim 18 or 20, wherein an amount of current that passes through the second current path is equal to or greater than an amount of current that passes through the first current path.

26. The semiconductor switching device of claim 18 or 20, wherein the second current path is formed to extend from an edge of the first impurity region by at least 10 μm.

27. The semiconductor switching device of claim 18 or 20, wherein the second current path is formed to extend from the bottom faces of the first and second high concentration impurity regions by at least 20 μm.

28. The semiconductor switching device of claim 18 or 20, wherein the second current path is configured to expand in response to an increase of the discharged electrostatic energy so as to increase a conductivity modulation efficiency of the second current path.

29. The semiconductor switching device of claim 18 or 20, wherein the first and second impurity regions are connected so as to increase an electrostatic breakdown voltage of the corresponding transistor by ten times or more from the electrostatic breakdown voltage of the corresponding transistor without the connection, a parasitic capacitance between the first and second impurity regions being 40 fF or smaller.

30. The semiconductor switching device of claim 19, 21 or 22, wherein a conductivity modulation efficiency of the third current path is at least 3 times higher than a conductivity modulation efficiency of the first current path of the protecting element without the second or third current path.

31. The semiconductor switching device of claim 19, 21 or 22, wherein the third current path is formed to extend from the extension part by at least 10 μm.

32. The semiconductor switching device of claim 19, 21 or 22, wherein the third current path is configured to expand in response to an increase of the discharged electrostatic energy so as to increase a conductivity modulation efficiency of the third current path.

33. The semiconductor switching device of claim 10, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and a width of the insulating region adjacent a back side face of one of the first and second high concentration impurity regions is 10 μm or larger, the back side face being opposite from a front

side face of said one of the first and second high concentration impurity regions which faces the part of the insulating region disposed between the first and second high concentration impurity regions.

34. The semiconductor switching device of claim 10, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and the insulating region extends from a side of the first or second high concentration impurity region by at least 10 μm, the side being substantially normal to sides of the first and second high concentration impurity regions facing each other through said portion of the insulating region.

35. The semiconductor device of claim 1, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and a width of the first impurity region is smaller than a width of the second impurity region so that upon discharging of an electrostatic energy through the protecting element a first current path for electron or hole is formed in the insulating region between opposing faces of the first and second high concentration impurity regions and between bottom faces of the first and second high concentration impurity regions and that a second current path for electron or hole is formed in the insulating region between the bottom face of the second high concentration impurity region and another side face of the fist high concentration impurity region, the second current path being deeper than the first current path.

36. The semiconductor device of claim 1, wherein the first and second high concentration impurity regions are embedded in the insulating region of the substrate and a width of the first impurity region is substantially equal to a width of the second impurity region so that upon discharging of an electrostatic energy through the protecting element a first current path for electron or hole is formed in the insulating region between opposing faces of the first and second high concentration impurity regions and between bottom faces of the first and second high concentration impurity regions and that a second current path for electron or hole is formed in the insulating region between the another side face of the second high concentration impurity region and another side face of the fist high concentration impurity region, the second current path being deeper than the first current path.

37. The semiconductor device of claim 35 or 36, wherein the width of the first high concentration impurity region is 5 μm or smaller.

38. The semiconductor device of claim 35 or 36, wherein the second current path is formed to extend from an edge of the first impurity region by at least 10 μm.

39. The semiconductor device of claim 35 or 36, wherein the second current path is formed to extend from the bottom faces of the first and second high concentration impurity regions by at least 20 μm.

40. The semiconductor device of claim 35 or 36, wherein the first and second impurity regions are connected so as to increase an electrostatic breakdown voltage of the corresponding transistor by ten times or more from the electrostatic breakdown voltage of the corresponding transistor without the connection, a parasitic capacitance between the first and second impurity regions being 40 fF or smaller.